

**In the Claims**

Please amend claims 1-20 as follows:

1. (Currently Amended) A structure, comprising:

an IC power distribution circuit;

a resistor electrically connected in series with the circuit;

an electrical switch electrically connected in parallel with the resistor; and

a controller comprising a timing circuit and a sequencer electrically connected to the timing circuit and the electrical switch, wherein the timing circuit is configured to generate, with a predetermined delay, a timing circuit trigger input signal to the sequencer, in response to an event signal which signifies an anticipated sudden change in power demand in the on-chip switching circuits, and wherein the sequencer is configured to open the electrical switch in response to the generation of the timing circuit trigger signal, the controller being electrically connected to the electrical switch and being configured to open the electrical switch to reduce the transient voltage variation across the circuit.

2. (Original) The structure of claim 1, wherein the controller is further configured to close the electrical switch at some time after the controller initially opens the electrical switch.

3. (Original) The structure of claim 2, further comprising one or a plurality of additional electrical switches, each electrically connected in parallel with the resistor and the first electrical switch, wherein each additional electrical switch is electrically connected to the controller.

BUR920030129US1  
SN 10707,171

4. (Canceled)

5. (Currently Amended) ~~The structure of claim 1, wherein the controller comprises:~~ A structure, comprising:

an IC power distribution circuit;

a resistor electrically connected in series with the circuit;

an electrical switch electrically connected in parallel with the resistor; and

a controller comprising a first comparator; and a sequencer electrically connected to the first comparator and the electrical switch, wherein the first comparator is configured to generate a first comparator trigger input signal to the sequencer, in response to the voltage across the power distribution circuit abruptly increasing, and wherein the sequencer is configured to open the electrical switch in response to the generation of the first comparator trigger signal, the controller being electrically connected to the electrical switch and being configured to open the electrical switch to reduce the transient voltage variation across the circuit.

6. (Original) The structure of claim 5, wherein the controller further comprises a second comparator electrically connected to the sequencer, wherein the second comparator is configured to generate a second comparator trigger input signal to the sequencer, in response to the voltage across the power distribution circuit abruptly decreasing, and wherein the sequencer is further configured to open the electrical switch in response to the generation of the second comparator trigger signal.

7. (Original) The structure of claim 1, wherein the electrical switch is a transistor.

BUR920030129US1  
SN 10707,171

8. (Original) The structure of claim 1, wherein the resistance of the electrical switch, while being closed, is substantially smaller than that of the resistor, and the resistance of the electrical switch, while being open, is substantially larger than that of the resistor.

9. (Currently Amended) A method for operating a structure, the method comprising the steps of:  
providing an IC power distribution circuit, a resistor electrically connected in series with the circuit, an electrical switch electrically connected in parallel with the resistor, and a controller electrically connected to the electrical switch; and

causing the controller to open the electrical switch to reduce the transient voltage variation across the circuit;

providing a timing circuit and a sequencer in the controller, the sequencer being electrically connected to the timing circuit and the electrical switch;

causing the timing circuit to generate, with a predetermined delay, a timing circuit trigger signal input to the sequencer, in response to an event signal which signifies an anticipated sudden change in power demand in the on-chip switching circuits; and

causing the sequencer to open the electrical switch in response to the generation of the timing circuit trigger signal.

10. (Original) The method of claim 9, further comprising the step of causing the controller to close the electrical switch at some time after the controller opens the electrical switch.

11. (Original) The method of claim 10, further comprising the steps of:

BUR920030129US1  
SN 10/707,171

providing one or a plurality of additional electrical switches, each electrically connected in parallel with the resistor and electrically connected to the controller;

causing the controller to open each additional electrical switch; and

causing the controller to later close each additional switch, after causing the controller to open each additional electrical switch.

12. (Canceled)

13. (Currently Amended) ~~The method of claim 9, further comprising the steps of:~~

A method for operating a structure, the method comprising the steps of:

providing an IC power distribution circuit, a resistor electrically connected in series with the circuit, an electrical switch electrically connected in parallel with the resistor, and a controller electrically connected to the electrical switch;

causing the controller to open the electrical switch to reduce the transient voltage variation across the circuit;

providing a first comparator and a sequencer in the controller, the sequencer being electrically connected to the first comparator and the electrical switch;

causing the first comparator to generate a first comparator trigger input signal to the sequencer, in response to the voltage across the power distribution circuit abruptly increasing; and

causing the sequencer to open the electrical switch in response to the generation of the first comparator trigger signal.

14. (Original) The method of claim 13, further comprising the steps of:

BUR920030129US1  
SN 10/707,171

5

providing, in the controller, a second comparator electrically connected to the sequencer;  
causing the second comparator to generate a second comparator trigger input signal to the  
sequencer, in response to the voltage across the power distribution circuit abruptly decreasing; and  
causing the sequencer to open the electrical switch in response to the generation of the  
second comparator trigger signal.

15. (Original) The structure of claim 9, wherein the electrical switch is a transistor.

16. (Original) The structure of claim 9, wherein the resistance of the electrical switch, while being  
closed, is substantially smaller than that of the resistor, and the resistance of the electrical switch,  
while being open, is substantially larger than that of the resistor.

17-20. (Canceled)